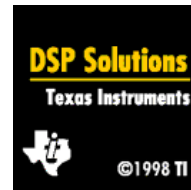




HUNT ENGINEERING
Chestnut Court, Burton Row,
Brent Knoll, Somerset, TA9 4BP, UK
Tel: (+44) (0)1278 760188,
Fax: (+44) (0)1278 760199,
Email: sales@hunteng.demon.co.uk
URL: <http://www.hunteng.co.uk>



We are a
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Traquair Data Systems Inc, 114 Sheldon Road, Ithaca, NY 14850 USA

Tel 607 266 6000, Fax 607 266 8221

Email Traquair@traquair.com, URL <http://www.traquair.com>

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HEGD2

16 Bit A/D GDIO Module

USER MANUAL

Hardware Rev B
Document Rev E
R.Williams 5/7/99

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TABLE OF CONTENTS

INTRODUCTION.....	4
MODULAR SYSTEMS	5
GDIO INTERFACE.....	6
CLOCK FREQUENCIES AND BANDWIDTH LIMITS	7
CAPABILITIES OF THE HEGD2	8
PHYSICAL LOCATION OF ITEMS ON THE HEGD2	9
GENERAL DESCRIPTION OF INTERFACES	10
RESET.....	10
CONFIG.....	10
WORD LENGTHS.....	11
PHYSICAL DIMENSIONS OF THE HEGD2	12
POWER REQUIREMENTS OF THE HEGD2.....	13
FITTING THE HEGD2 TO A MODULE CARRIER.....	14
SOFTWARE REQUIREMENTS	15
CONNECTOR PIN-OUTS	16
ANALOGUE INPUT CONNECTORS	16
`SAMPLE CLOCK' CONNECTOR	16
DATA FORMAT.....	18
CHANNEL SEQUENCES	19
SAMPLE FREQUENCIES.....	20
USER OSCILLATOR SOCKET.....	21
JUMPER SETTINGS AND SAMPLE FREQUENCY.....	22
A/D INPUT STAGE	23
CE MARKING.....	24
TECHNICAL SUPPORT	25

The HEGD2 is a 16-bit A/D GDIO module for use in HUNT ENGINEERING's real-time DSP systems. It provides A/D conversion for up to 2 groups of four simultaneously sampled analogue input channels.

The HEGD2 uses the Crystal Semiconductor CS5101A 16-bit, 100kHz A/D converter. The CS5101A converter can digitise either one or two analogue inputs at a maximum rate of 100kHz or 50kHz. The HEGD2 uses four converters, providing either four or eight channels of analogue to digital conversion. In four-channel operation the HEGD2 provides one channel per A/D at up to 100kHz per channel. In eight-channel operation the HEGD2 provides two channels per A/D at up to 50kHz per channel.

The digital output of the converters is latched and written to the FIFOs of the GDIO interface of the supporting subsystem.

There is no processor on the HEGD2. The converters and data latches are controlled by an FPGA. The FPGA operates in two modes. In four-channel operation the FPGA presents A/D data from channels A, B, C and D of the HEGD2. In eight-channel operation the FPGA presents A/D data from all channels, A to H. A single jumper sets the mode of operation.

The A/D sample clock can be sourced from the crystal oscillator site on the HEGD2, or from an external clock signal connected to the 'Sample Clock' header. The crystal oscillator can also be used to drive the external clock input of further HEGD2 modules.

When using the module's crystal-oscillator, the crystal frequency is divided by a factor of 160 before driving the sample clock input of the A/D converters. The divided signal is placed on the 'Sample Clock' header for connecting to other modules. When using the external clock input with the 'Sample Clock' header, the external clock is connected directly to the A/Ds.

The falling edge of the sample clock input will cause all of the A/D converters to hold and begin conversion on the input channels. If the HEGD2 is in four channel mode, each falling edge will hold the four input channels A, B, C and D, converting these four channels simultaneously. If the HEGD2 is in eight channel mode, each alternate falling edge will cause a group of four channels to be sampled and held simultaneously. The first falling edge of the sample clock will cause channels A, B, C and D to be held and simultaneously converted. The next falling edge will cause channels E, F, G and H to be held and simultaneously converted. In this way there is a finite delay between the point at which samples are taken from the first group of four inputs and the second group of four inputs. This time difference is equal to one sample clock period.

The HEGD2 is an I/O module to be used in a modular system. Because this means that the use of the module can be very varied, it is necessary to read this user manual in conjunction with the user manuals of any other products being used in the system.

If you have discussed with us how you will use your system, then it is likely that we have provided a separate “system” manual that attempts to describe how the components are connected and can be used in your particular configuration.

If you did not receive such a system description then it is probably because we did not have enough information to know how that system was to be used. The software examples in the directories under **\software\boards\hegd2** on the HUNT ENGINEERING CD should be able to guide you. To view this software select “view software” from the CD index page.

If you still have problems understanding or using your HEGD2 contact us as described in the Technical Support section of this manual.

The GDIO interface is a simple FIFO based interface. It assumes that there are synchronous FIFOs on the module carrier card that are clocked and controlled by the logic on the GDIO module.

There is separate input and output FIFOs, connected to the module using two separate 16-bit data busses, plus the relevant FIFO control signals.

For full details of the GDIO interface refer to the "HERON module specification" available on the HUNT ENGINEERING CD or web site. This document provides all of the information about the GDIO and HERON module interfaces. (HERON is a super-set of the GDIO module).

HUNT ENGINEERING is happy for our customers to use this document to design their own HERON or GDIO modules, or to design their own carrier cards for these modules.

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Clock Frequencies and Bandwidth Limits

The HEGD2 provides a clock to the GDIO output FIFO that is 18.432Mhz. Although this implies a theoretical data rate over the 16 bit interface of 36.864 Mbytes/second, this is not actually achievable because of the speed of the A/Ds. The actual rate achieved depends on the mode (4 channel or 8 channel) and the actual sample frequency used.

Capabilities of the HEGD2

The HEGD2 provides a means of digitising up to 8 channels of analogue data for use with HUNT ENGINEERING's real time DSP systems. The '4/8' jumper provides a choice of four or eight channel operation. All 8 channels have an input stage that performs low-pass filtering and gain on the input.

The HEGD2 has a 5-pin header labelled 'Sample Clock' that can be used to connect an external sample clock to the module, or to drive the modules own sample clock and other connected HEGD2 GDIO modules.

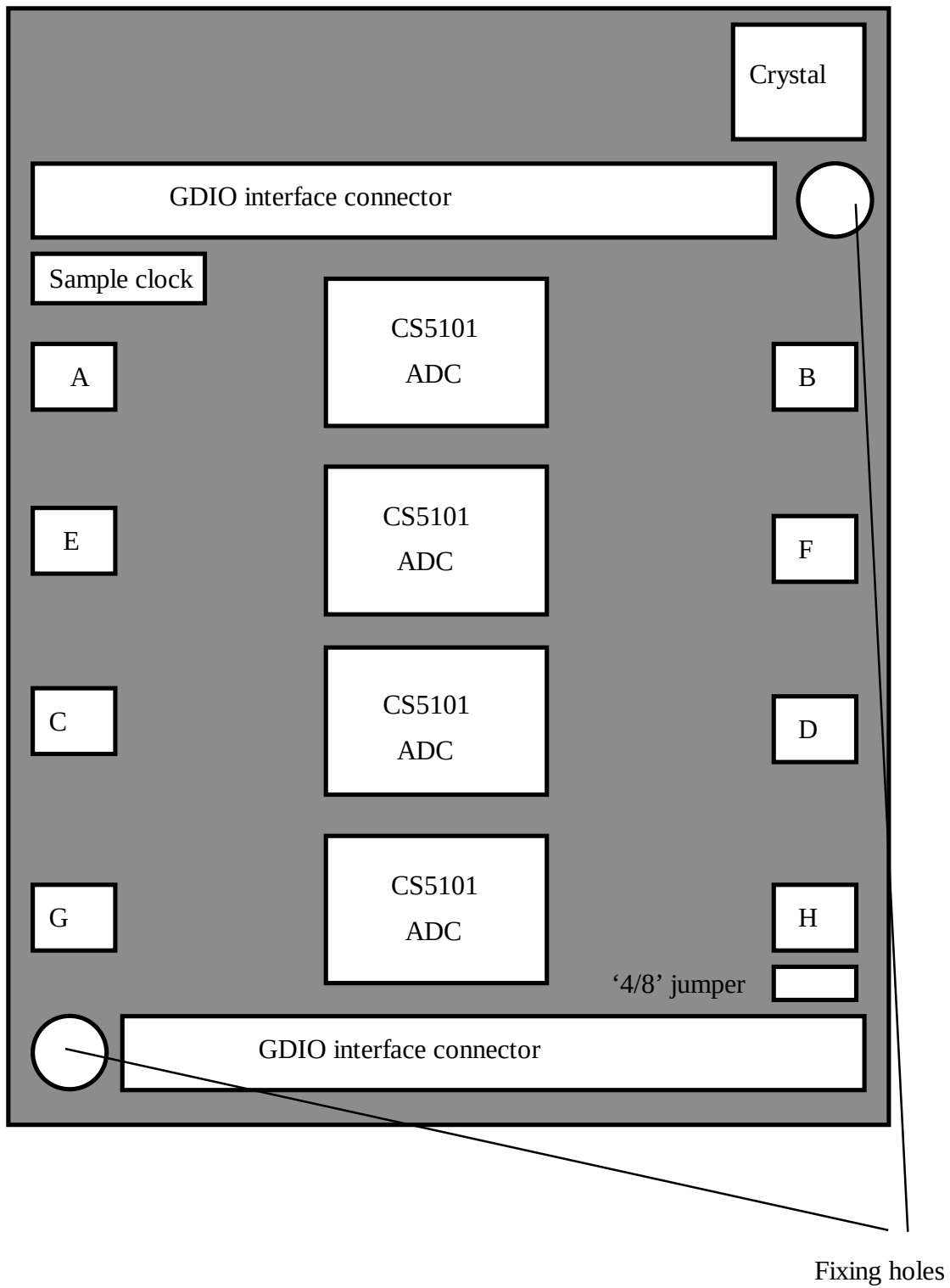
A 'user' crystal oscillator socket is mounted on the HEGD2 to allow the sample frequency to be set as required. To align the available range of crystal oscillators with the sample frequencies used by the A/Ds the crystal oscillator output frequency is divided by 160 before the Sample Output pin on the 'Sample Clock' header. This output is adjacent to the External Sample Input so that the two can be linked with a jumper. The 'Sample Clock' input is buffered by the HEGD2.

The CS5101A converter works in bipolar mode, where an input voltage above +VREF will produce an output of all 1's and an input voltage below -VREF will produce an output of all 0's. The converter outputs data in binary form. The following table shows the output coding of the CS5101A. The voltage reference is 4.5V.

Binary Data Out	Input Voltage (after Input Stage)
FFFF	$> (+4.5 - 1.5 \text{ LSB})$
FFFF	$+4.5 - 1.5 \text{ LSB}$
FFFE	$+4.5 - 1.5 \text{ LSB}$
8000	-0.5 LSB
7FFF	-0.5 LSB
0001	$-4.5 + 0.5 \text{ LSB}$
0000	$-4.5 + 0.5 \text{ LSB}$
0000	$< (-4.5 + 0.5 \text{ LSB})$

Table 1 (One LSB is equivalent to 0.137 mV)

Physical Location of Items on the HEGD2



General Description of Interfaces

The HEGD2 will work with all boards that implement the HUNT ENGINEERING GDIO interface. This includes all HERON module carrier. Details of the HERON specification can be found on the HUNT ENGINEERING CD or web site, www.hunteng.co.uk.

Reset

The first level of Reset on the HEGD2 is a single reset pin that must be taken low to assert the reset and taken high to de-assert the reset. This signal must be driven at all times, as the hardware will not function predictably with this signal floating.

Config

The CONFIG signal is active (low) on reset and is primarily used to disable any I/O to or from the GDIO interface until system processor modules have booted and are ready to accept A/D data. Refer to the relevant carrier board manual for details of how to do this.

The HEGD2 uses the 16 bit GDIO FIFO to store its samples into.

Often GDIO module carriers implement a 32 bit FIFO to store two data items from the GDIO interface in the same 32-bit word.

HERON module carriers always have a 32 bit FIFO and store two 16-bit data items from the GDIO interface in the same 32 bit word.

The user manual for the carrier board used should always be referred to for details, but normally the order of the data items is guaranteed to be low half of 32 bit word first, followed by the top half. This guarantees the time ordering of the samples.

The HEGD2 uses the GDIO FIFO to store 32 bit samples into, and always guarantees that the two halves of the 32 bit word are correctly ordered even after a FIFO overflow.

When a FIFO overflow occurs, an unknown number of 32 bit words are lost, but unlike some GDIO modules, the ordering of the two 16 bit half words is maintained.

For this reason it is usual to check the channel identifier bits in the data to determine which channel the data originates from. See the example software in the directories under **\software\boards\hegd2** on the HUNT ENGINEERING CD. Select view software from the CD index.

Physical Dimensions of the HEGD2

The GDIO module is 4.0 inches x 2.5 inches (101mm x 63.5mm) and is mounted above the module carrier with a board to board spacing of 5mm. The maximum height of components above the HEGD2 is 9mm.

Cable connectors will increase the space required above the HEGD2. As a guide an IDC connector on the channel input connector increases the component height to 14mm, while a Du Pont connector will increase the height to about 25mm.

Power Requirements of the HEGD2

The HEGD2 uses the following voltage supplies:

Power Lines Used
+5V supply
+12V supply
-12V supply

Table 2. *Power Lines Used.*

The current requirement of the HEGD2 is shown in table 3.

Power Line	Maximum	Typical
+5V	650 mA	550 mA
+12V	120 mA	80 mA
-12V	120 mA	80 mA

Table 3. Power consumption of the HEGD2

Fitting the HEGD2 to a Module Carrier

Care must be taken when fitting the HEGD2 to a module carrier. Ensure that the HEGD2 is the right way round and correctly aligned. To assist in correct alignment, the GDIO board outline is marked on the hosting board.

The HEGD2 should only be fitted when there is no power applied to the Motherboard. Only light pressure need be exerted over each connector to force it fully home. Take care not to apply excessive pressure to the centre of either PCB as this could stress the PCB unnecessarily. If the environment demands positive retention of the modules, fixing holes are provided for nylon M3 retention bolts. Refer to relevant carrier board manual for specific fixing details.

Normal anti-static precaution procedures should be followed at all times.

Software Requirements

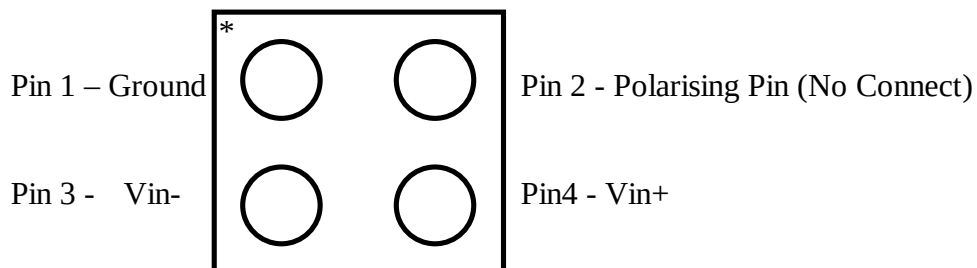
There are a few requirements that the hardware places on the Software to enable the HEGD2 to function correctly. It is important de-assert the CONFIG line on all processor modules in the system as the on-board logic is held in a reset state all the time that CONFIG is asserted. This is to prevent HEGD2 data interfering with processor boot sequences.

It is important to remember that the HEGD2 continuously digitises signals at the rate defined by the sampling clocks. If the data is not read from the hosting board's GDIO interface at a fast enough rate then the buffering FIFO will become full and data will be lost. If the FIFO does become full then care must be taken when starting to read data again as the data stored on the processor and GDIO FIFO may contain missing samples. When running in four or eight channel operation, each word should contain a sample in the bottom 16 bits of the word, and a channel I.D in the next 3 bits (bits 16-18) of the word. By looking for the presence of the expected sequence of channel IDs in received words, software can check that data is being received correctly. In four channel operation for example, the channel I.D should cycle from 0 to 3 every four words, and in eight channel operation the channel I.D should cycle from 0 to 7 every eight words.

Support software is available on the HUNT ENGINEERING CD. Select view software from the CD index. In the \software\boards\hegd2 directory there are directories containing sample software for the HEGD2.

Analogue Input Connectors

The pin-out of the eight analogue inputs is shown below. (An asterisk marks pin 1 on the board.)

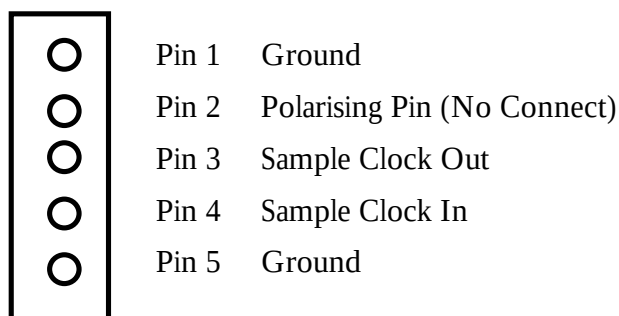


The HEGD2 provides a differential front-end with each channels input stage. The connector shown above provides two signal pins in order to connect a differential input to the HEGD2. When connecting a single-ended input to the HEGD2, connect the single-ended input to the Vin+ pin and connect its associated ground to the Vin- pin. If measurement of the DC offset in the signal is required, then the Vin- signal should be connected to the board ground (pin 1), as well as the signal ground.

The 'Input x' headers will accept many connector types. An example of a suitable connector is the Du Pont 65043-035 housing, with Du Pont 47712-002 crimps. Note the HEGD2 has an asterisk on the silk screen to indicate the location of pin 1. As in the diagram above, pin 1 corresponds to Ground.

'Sample Clock' Connector

The HEGD2 provides a 5-pin header for connecting sample clocks between modules. The sample clock derived from the custom crystal oscillator and divide by 160 logic can be used to drive the sample clock in of another HEGD2. Conversely, the HEGD2 sample clock in can be driven by another HEGD2.



The 'Sample Clock' header will accept many connector types. An example of a suitable connector is the Du Pont 65039-32 housing, with Du Pont 47712-002 crimps. Note, the HEGD2 has a box on the silk screen to indicate the location of pin 1.

The maximum sample clock frequency that can be applied to the HEGD2 is 100kHz. This frequency will provide 100kHz sampling in four channel mode, and 50kHz sampling in eight channel mode.

The HEGD2 operates in either four-channel operation or eight-channel operation. When the '4/8' jumper is not fitted, the HEGD2 is in four channel mode. In this mode the module produces 4 words of data every sample clock cycle. The 4 words of data contain the digitised data from channels A, B, C and D. Each sample is transferred using the 16-bit wide GDIO slot interface as one 32 bit word. The bottom 16-bits of the word contains the sample data, and the top 16-bits contains a 3-bit channel ID. The sequence of data output over the GDIO interface would be as follows for one sample clock cycle.

	Bits 19-31	Bit 18	Bit 17	Bit 16	Bits 15-0
1st word transmitted	Undefined	0	0	0	Sampled data - channel A
2nd word transmitted	Undefined	0	0	1	Sampled data - channel B
3rd word transmitted	Undefined	0	1	0	Sampled data - channel C
4th word transmitted	Undefined	0	1	1	Sampled data - channel D

When the '4/8' jumper is fitted the HEGD2 is in eight channel mode. In this mode the module produces 8 words of data every two sample-clock cycles. The first sample clock cycle produces digitised data from channels A, B, C and D. The second sample clock cycle produces digitised data from channels E, F, G and H. Each sample is transferred to the GDIO interface in one 32-bit word. The bottom 16-bits of the word contains the sample data, and the top 16-bits contains a 3-bit channel ID.

	Bits 19-31	Bit 18	Bit 17	Bit 16	Bits 15-0
1st word transmitted	Undefined	0	0	0	Sampled data - channel A
2nd word transmitted	Undefined	0	0	1	Sampled data - channel B
3rd word transmitted	Undefined	0	1	0	Sampled data - channel C
4th word transmitted	Undefined	0	1	1	Sampled data - channel D
5th word transmitted	Undefined	1	0	0	Sampled data - channel E
6th word transmitted	Undefined	1	0	1	Sampled data - channel F
7th word transmitted	Undefined	1	1	0	Sampled data - channel G
8th word transmitted	Undefined	1	1	1	Sampled data - channel H

Channel Sequences

The sequence of the channels sampled depends on the setting of the 4/8 jumper.

As shown above, in 4 channel mode the sequence is A,B,C,D.

As shown above, in 8 channel mode the sequence is A,B,C,D,E,F,G,H

Sample Frequencies

The maximum sample frequency is dependent on the number of channels selected, this is a function of the A/D chips used by the HEGD2.

The maximum sample frequencies are:

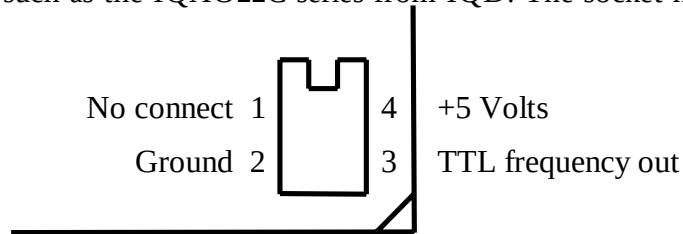
4 Channel:	100 KSamples/sec
8 Channel:	50 KSamples/sec

These are the rates that can be obtained when the internal trigger is used and are as fast as the converter can achieve. An external trigger must be used to obtain frequencies other than these, and the external trigger frequency must be less than or equal to the maximum frequencies shown above.

The channels selected are sampled in two simultaneous groups, channels A, B, C and D on the rising edge, and E, F, G, and H on the falling edge of the trigger.

User Oscillator Socket

There is a socket provided for an oscillator module, which is divided by 160 before being connected to the sample clock out connector. The socket is designed to accept plastic bodied type oscillators such as the SG531 type from Seiko Epson. The package is a 0.3" 8 pin DIL type body but with only 4 pins. A more conventional type of oscillator module in metal packing could also be used, such as the IQXO22C series from IQD. The socket has four pins as shown below:



When using the custom crystal oscillator and divide by 160 logic on the HEGD2 to drive the sample clock, a jumper should be fitted between pins 3 and 4 of the 'Sample Clock' connector. This will directly connect the crystal oscillator output (after being divided by 160) to the sample clock of the module.

When using the custom crystal oscillator to drive both this HEGD2 and other HEGD2 sample clocks, the Sample Clock Out (pin 3) of this module should be connected to both the Sample Clock In (pin 4) of this module, as well as the Sample Clock In of the other HEGD2 modules.

When using an external sample clock, the external clock should be connected to the Sample Clock In (pin 4) of this module and the Sample Clock Out (pin 3) should be left unconnected. The sample clock in is buffered onto the module, presenting one TTL load. e.g.

I_{ih} 20uA at 2.7V
 I_{il} -0.1mA at 0.4V

The Sample clock out is driven by F logic, and hence has the following characteristics

V_{oh} (I_{oh} -1mA) = 2.7V
 V_{ol} (I_{ol} 20mA) = 0.5V

Jumper Settings and Sample Frequency

The HEGD2 has one jumper that defines the number of channels digitised. With the '4/8' jumper removed, the HEGD2 works in four channel mode. In this mode, the clock frequency applied to the 'Sample Clock In' pin of the 'Sample Clock' connector is the sample clock used by all A/D converters. The maximum frequency that can be applied to this input is 100kHz, which will provide four channels at 100kHz sampling per channel.

With the '4/8' jumper fitted, the HEGD2 works in eight channel mode. In this mode, the clock frequency applied to the 'Sample Clock In' pin is equivalent to twice the sample frequency used by the A/D converters. When in eight channel operation, the HEGD2 uses alternate sample clock cycles to digitise first channels A, B, C and D, and second channels E, F, G and H. The maximum frequency that can be applied to the sample clock input is 100kHz. With the 'Sample Clock In' at 100kHz, the HEGD2 will digitise all 8 channels in two cycles. This results in eight channels at 50kHz sampling per channel. In addition the phase difference between each group of sample (A to D, and E to H) is equal to one 'Sample Clock In' cycle.

Each analogue input of the HEGD2 has an input stage that comprises of a differential input stage and a low pass filter stage. The standard settings of the HEGD2 provide an overall input gain of 1, with a low pass filter bandwidth of 50kHz. Each input has an input impedance of 1KOhms. If required each of these parameters can be altered at build time to provide the required input gain, low pass filter bandwidth and input impedance.

Default parameters

DIGITISATION RANGE:	+ / - 4.5 Volts
INPUT IMPEDANCE:	1k Ohms
GAIN TO A/D:	1
SMALL SIGNAL BANDWIDTH:	50KHz

The channel inputs are differential and the absolute maximum input should not exceed + / - 8 Volts. To prevent possible accidental damage the input stage has protection diodes.

The zero input noise in an HEGD2 will typically cause the digitised output of a channel input shorted to ground to spread over more than one digitisation level. Typically under these conditions 95% of the digitised outputs will be within four adjacent levels. The crosstalk between channels of an HEGD2 does not exceed the zero input noise.

HUNT ENGINEERING have performed testing on its products to ensure that it is possible to comply with the European CE marking directives. The HEGD2 cannot be CE marked as it is a component in a system, but as long as the following recommendations are followed, a system containing the HEGD2 could be CE marked.

The immense flexibility of the HUNT ENGINEERING product range means that individual systems should be marked in accordance with the directives after assembly.

1.The host computer or housing in which the HEGD2 is installed is properly assembled with EMC and LVD in mind and ideally should itself carry the CE mark.

2.Any cabling between boards or peripherals is either entirely inside the case of the host computer, or has been assembled and tested in accordance with the directives. The HEGD2 inputs are NOT protected against Static discharge, so if the cabling does exit the case, suitable protection must be added elsewhere in the system.

HUNT ENGINEERING are able to perform system integration in accordance with these directives if you are unsure of how to achieve compliance yourself.

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