

CIO-DDA06/Jr

Analog Output
&
Digital I/O

User's Manual



**MEASUREMENT
COMPUTING™**

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MEGA-FIFO, the CIO prefix to data acquisition board model numbers, the PCM prefix to data acquisition board model numbers, PCM-DAS08, PCM-D24C3, PCM-DAC02, PCM-COM422, PCM-COM485, PCM-DMM, PCM-DAS16D/12, PCM-DAS16S/12, PCM-DAS16D/16, PCM-DAS16S/16, PCI-DAS6402/16, Universal Library, *InstaCal*, *Harsh Environment Warranty* and Measurement Computing Corporation are registered trademarks of Measurement Computing Corporation.

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1. INTRODUCTION

1.1 GENERAL DESCRIPTION

The CIO-DDA06/JR can have a maximum of six analog ± 5 Volt output channels (two are installed) and 24 digital inputs and/or outputs. The analog outputs are dual-DAC AD7237s. The CIO-DDA06/JR is 100% register-compatible with the CIO-DDA-06.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. Since the control register is double buffered, the DAC's output is not updated until both bytes (first low byte, then high byte) have been written to the DAC control.

The analog outputs may also be set for simultaneous update in groups of two, four or all six. Analog outputs are grouped as 0 and 1, 2 and 3, and 4 and 5. By selecting XFER on the jumper beside the DAC, each pair can be set for simultaneous transfer.

When a DAC pair is set for simultaneous transfer, writing new digital values to the DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ from one of the board's addresses (any address base + 0 through base + 11).

In this way the CIO-DDA06/JR may be set to hold new values until all channels are loaded, then update any two, any four, or all six channels simultaneously. This is a very useful feature for multi-axis motor control.

The CIO-DDA06/JR digital I/O lines are an emulation of the 82C55 chip in mode 0. The digital I/O is equivalent to a CIO-DDIO24H, high drive digital I/O board. This is sufficient to switch other TTL or similar inputs, as well as relays, LEDs or solid state relays.

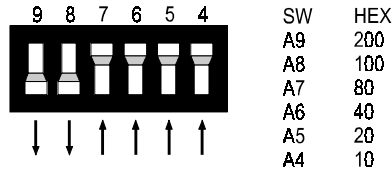
2. SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *InstaCal*[™] program provided with your board. Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *InstaCal*[™]. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *InstaCal*[™] and/or your computer.

3. HARDWARE INSTALLATION

3.1 BASE ADDRESS

The CIO-DDA06/JR is I/O mapped and occupies 16 eight-bit addresses in the PC. The first (BASE) address is controlled by a DIP switch.



BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3.1 Base Address Switch

Set the switches on your base address switch as shown in Figure 3-1. Unless there is already a board in your system which uses address 300h (768 decimal) leave the switches as they are set at the factory.

In the example in Figure 3-1, the CIO-DDA06/JR is set for base address 300h (768 decimal).

3.2 SIMULTANEOUS TRANSFER JUMPER

The analog outputs may be jumpered so that new output data are held until all desired DACs have been loaded with new digital data, then, as a group, all new data updates the voltage outputs. The simultaneous transfer occurs when any addresses BASE + 0 through BASE + B are read.

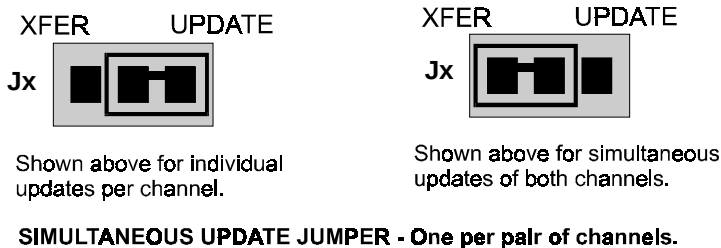


Figure 3-2. Simultaneous XFER/Individual UPDATE Jumper

The analog output chips are dual DACs. There are two analog outputs are on each chip. A single jumper sets both DACs on a single chip to be either simultaneous TRANSFERS or individual UPDATES (Figure 3-2).

Figure 3-2 shows the jumper in each configuration. If you look at the board, you will see the jumpers are labeled J1, J2, or J3 next to each jumper:

- J1 sets the transfer mode for the channels 0 & 1,
- J2 sets the transfer mode for the channels 2 & 3,
- J3 sets the transfer mode for the channels 4 & 5.

3.3 BOARD INSTALLATION

1. Turn the power off.
2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.
3. Locate an empty expansion slot in your computer.
4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DDA06/JR.

3.4 CABLING

The connector is accessible through the PC/AT expansion bracket. The connector is a standard 37-pin male connector. The signal levels and pin assignments are identical with the CIO-DDA06. Pin assignments of the 24 digital bits are identical with the CIO-DIO24 and 24H.

Several cabling and screw termination options are available:

DFCON-37	D-connector, D-shell and pins to construct your own cable.
C37FF-#	2-foot (and longer) ribbon cable with 37-pin D-connectors.
C37FFS-#	5-foot and 10-foot shielded round cable with molded ends housing 37-pin connectors.
CIO-MINI37	Simple, 40-position 4 x 4 in. screw terminal board.
CIO-TERMINAL	Full-featured 4x16in. screw terminal board with prototyping and interface circuitry.
SSR-RACK24	24-position Solid State Relay mounting and interface board.
ISO-RACK08	8-position Isolated Analog Module mounting and interface board.
ENC-MINI37	Enclosure for the MINI37.
ENC-17-3	Enclosure for larger external accessory boards.

3.5 SIGNAL CONNECTIONS

ANALOG

The analog outputs of the CIO-DDA06/JR are two-wire hook-ups. A signal, labeled D/A # OUT on the connector diagram below, and a Low Level Ground (LLGND). The low level ground is analog ground.

NOTE: Use LLGND as the ground reference for all analog hook-ups.

The output range of the CIO-DDA06/Jr is ± 5 volts and cannot be changed. There are no trimming pots on the board so no hardware calibration is necessary or possible.

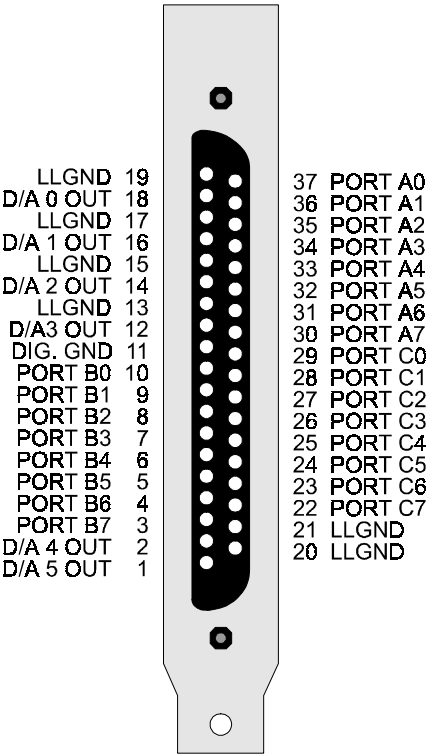
DIGITAL

All the digital inputs/outputs on the CIO-DDA06/JR connector are TTL level. Under normal operating conditions, the voltages range from near 0 volts for the low state to near 5 volts for the high state. In the low state, the digital output can sink 64 mA. In the high state, the digital output can source 15 mA.

3.6 CONNECTOR DIAGRAM

The CIO-DDA06/JR connector is a 37-pin D-type connector accessible from the rear of the PC through the expansion backplate (Figure 3-3). The connector accepts female 37-pin D-type connectors, such as on the C37FF-2, a 2-foot cable.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL, CIO-SPADE50 and CIO-MINI37 screw terminal boards.



37 PIN CONNECTOR - Pin assignments of 8255 digital signals are identical to CIO-DIO24.

Figure 3-3. 37-Pin Connector Pin-out

4. REGISTER ARCHITECTURE

The CIO-DDA06/JR is a simple board to understand. All control and data is read/written with simple I/O read and write signals. No interrupt or DMA control software is required. Hence, the board's functions are easy to control directly.

4.1 REGISTER OVERVIEW

There are 12 analog output registers. There are two registers for each channel, one for the lower eight bits and one for the upper four bits. An additional four addresses are occupied by the three digital I/O data registers and one control register. The board occupies a total of 16 I/O addresses.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

The numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte.

The method of programming required to set/read bits from bytes is beyond the scope of this manual.

In summary form, the registers and their function are listed on Table 4-1. Within each register are eight bits which may constitute a byte of data or eight individual bit set/read functions.

Table 4-1. Board Registers

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous update
BASE + 1	D/A 0 Most Significant Nibble	Initiate simultaneous update
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous update
BASE + 3	D/A 1 Most Significant Nibble	Initiate simultaneous update
BASE + 4	D/A 2 Least Significant Byte	Initiate simultaneous update
BASE + 5	D/A 2 Most Significant Nibble	Initiate simultaneous update
BASE + 6	D/A 3 Least Significant Byte	Initiate simultaneous update
BASE + 7	D/A 3 Most Significant Nibble	Initiate simultaneous update
BASE + 8	D/A 4 Least Significant Byte	Initiate simultaneous update
BASE + 9	D/A 4 Most Significant Nibble	Initiate simultaneous update
BASE + 10	D/A 5 Least Significant Byte	Initiate simultaneous update
BASE + 11	D/A 5 Most Significant Nibble	Initiate simultaneous update
BASE + 12	Port A Output	Port A Input
BASE + 13	Port B Output	Port B Input
BASE + 14	Port C Output	Port C Input
BASE + 15	Configure digital I/O	None.

4.2 DIGITAL DATA REGISTERS

D/A 0 LEAST SIGNIFICANT 8 BITS

BASE ADDRESS + 0

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12

LSB

D/A 0 MOST SIGNIFICANT 4 BITS

BASE ADDRESS + 1

7	6	5	4	3	2	1	0
X	X	X	X	D1	D2	D3	D4

MSB

Writing data to the LSB loads that data into the D/A load register but does not update the D/A output. Writing data to the MSB both loads the upper four bits of the 12 bit digital value and updates the output of the D/A.

The function and bit layout of the remaining 10 D/A registers (5 D/As) is identical to that shown above.

PORT A DATA

BASE ADDRESS + 12

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA

BASE ADDRESS + 13

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B may be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes the individual bits are used.

Note that bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA

BASE ADDRESS + 14

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C may be used as one 8-bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4-bit port is CH3 - CH0, and for the lower, CL3 - CL0.

Although it can be split, reads and writes to port C carry eight bits of data so unwanted data must be ANDed out of reads, and OR'd out of writes.

OUTPUT PORTS

Ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS

Ports configured for input read the state of the input lines at the moment the read is executed. Transitions are not latched.

4.3 DIGITAL CONTROL REGISTER

BASE ADDRESS + 15

7	6	5	4	3	2	1	0
X	X	X	A	CH	X	B	CL

A	B	CL	CH	INDEPENDENT FUNCTION
1	1	1	1	Input
0	0	0	0	Output

The Ports A, B, C High and C Low may be independently programmed for input or output. The control register responds to the same control codes as the 82C55 in Mode 0. The codes for configuring in the board are given in Table 4-2 below.

Table 4-2. CIO-DDA06/Jr - Digital I/O Configuration Coding

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

NOTE: D7 is always (1). D6, D5, and D2 are always (0).

5. SPECIFICATIONS

Typical for 25°C unless otherwise specified.

POWER CONSUMPTION

+5V Supply	650 mA typical / 1196 mA max.
+12V Supply	33 mA typical / 45 mA max. (for each pair of D/A channels installed)
–12V Supply	9 mA typical / 15 mA max. . (for each pair of D/A channels installed)

The +12V and –12V supply current values shown are when two D/A channels are installed. Additional channels increase the $\pm 12V$ currents but have no affect on the +5V supply current consumption.

ANALOG OUTPUTS

D/A type	Dual DAC, AD7237
Resolution	12 bits (1 part in 4096 or 0.0244% F.S.)
Channels	6 max. Two are installed, add more by pairs
Output Range	$\pm 5V$

Offset error	± 3 LSB
Gain error	± 5 LSB
Differential Nonlinearity	± 0.9 LSB
Integral Nonlinearity	± 0.5 LSB
Monotonicity	Guaranteed

D/A pacing	Software paced
D/A trigger modes	Software
Data transfer	Programmed I/O
Throughput	PC dependent
Settling time (10V step to .01%)	5 μ s typ, 10 μ s max
Slew rate	3V/ μ s

Current Drive	± 5 mA min
Output short-circuit duration	80 mA typ
Output resistance	<0.5 ohm

Miscellaneous	Double buffered output latches Update DACs individually or simultaneously (jumper selectable)
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DIGITAL I/O

Digital Type	8255 emulation
Output:	74S244
Input:	74LS373
Number of I/O	24
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Output high	2.4V min @ -15 mA
Output low	0.5V max @ 64 mA
Input high	2.0V min, 7V max
Input low	-0.5V min, 0.8 V max
Power-up / reset state	Input mode (high impedance)

ENVIRONMENTAL

Operating Temperature	0 to 70 deg C
Storage Temperature	-40 to 100 deg C
Humidity	0 to 90% non-condensing

For Your Notes

For Your Notes

For Your Notes

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

<u>CIO-DDA06/Jr</u>	<u>Analog output and digital I/O card</u>
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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