

CIO-CTR10HD & CIO-CTR20HD



**MEASUREMENT
COMPUTING™**

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MEGA-FIFO, the CIO prefix to data acquisition board model numbers, the PCM prefix to data acquisition board model numbers, PCM-DAS08, PCM-D24C3, PCM-DAC02, PCM-COM422, PCM-COM485, PCM-DMM, PCM-DAS16D/12, PCM-DAS16S/12, PCM-DAS16D/16, PCM-DAS16S/16, PCI-DAS6402/16, Universal Library, *InstaCal*, *Harsh Environment Warranty* and Measurement Computing Corporation are registered trademarks of Measurement Computing Corporation.

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1 INTRODUCTION

The CIO-CTR##HD##HD is really a single board with two CIO-CTR05's on it. For the balance of this manual we will refer to both boards as the CIO-CTR##HD, and will only use the complete board name in instances where there are items specific to one board or the other.

The CIO-CTR family is fully supported by the powerful Universal Library package. Details regarding installation and usage of the Universal Library software can be found in the Universal Library documentation. Please note that InstaCal (shipped with the board) creates a configuration file required for programmers who use the Universal Library programming libraries.

2 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *InstaCal*[™] program provided as part of your software package. *InstaCal*[™] will show you all available options, how to configure the various switches and jumpers (as applicable) to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *InstaCal*[™]. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *InstaCal*[™] and/or your computer.

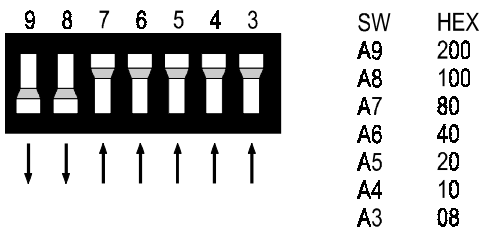
3 HARDWARE INSTALLATION

We highly recommend that you use the InstaCAL procedure to guide you through setting up your board. However, the following sections are provided in case you need to set up your board and you do not have access to the InstaCAL program.

The CIO-CTR##HD has one bank of switches, a base address switch, and one jumper block which must be set before installing the board in your computer.

3.1 BASE ADDRESS

Unless there is already a board in your system which uses address 300h (768 Decimal) then you can leave the switches as they are set at the factory.



In the example shown here, the CIO-CTR##HD is set for base address 300h (768 Decimal).

BASE ADDRESS SWITCH - Address 300H shown here.

Certain address are used by the PC, others are free and can be used by the CIO-CTR##HD and other expansion boards. We recommend trying BASE = 300h (768D) first.

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0AF	8259 PIC #2 (AT)	320-31F	HARD DISK (XT)
0A0-0A1	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-CTRHD BASE switch may be set for address in the range of 000-3F8 so it should not be hard to find a free address area for your CIO-CTRHD. Once again, if you are not using IBM prototyping cards or some other board which occupies these

addresses, then 300-31F HEX are free to use. Address not specifically listed, such as 390-39F, are usually free.

3.2 INTERRUPT LEVEL SELECT

A single interrupt input at pin 26 allows you to initiate an interrupt service routine with an external pulse. The interrupt level is selected via software and is one of the options set in the InstaCal configuration file.

3.3 CLOCK SOURCE SELECT

The source of the pulses supplied to the 9513 for timing operations is programmable and there are a number of options. These options are shown in the InstaCal INSTALL screen.

3.4 INSTALLING THE CIO-CTR##HD IN THE COMPUTER

Turn the power off. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

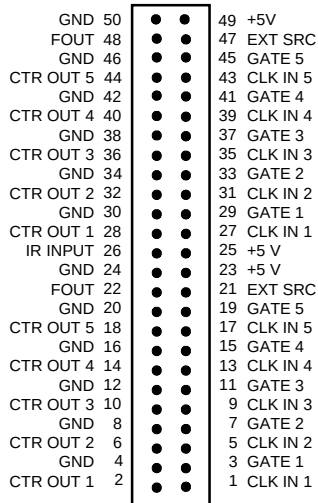
Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-CTRHD.

The CIO-CTRxxHD connector is a 50 pin header type connector. All the signals from the 9513 and interrupt are accessible. Pin one is designed by a square solder pad. It is the pin on the PC Bus end of the connector, and closest to the edge of the card.

Cables C50FF-2 and the CIO-MINI50 allow easy connection to all of the counter signals through 12-22 AWG screw terminals. The CIO-CTR20HD has two of these connectors, P1 and P2. The signals on each are identical.

4 I/O CONNECTOR & PINOUT

The CIO-CTRxxHD use a 50-pin inline connector. The CIO-CTR10HD has only one connector while the CIO-CTR20HD has two. The connectors are compatible with the optional C50FF-series cables and CIO-MINI50 screw terminal adapter board. The pinout of these connectors is shown below.



CIO-CTRxxHD CONNECTOR

NOTE:

Chip 1 (U1) is accessed at the bottom half of P1 (pins 1 - 22);
 Chip 2 (U2) is the top half of P1 (pins 27 - 48);
 Chip 3 (U3) is accessed at the bottom half of P2 (pins 1 - 22);
 Chip 4 (U4) is the top half of P2 (pins 27 - 48).

5 REGISTER MAP

5.1 CONTROL & DATA REGISTERS

The CIO-CTR10HD is composed of two AM9513 counter timer chips, the CIO-CTR20HD is composed of four. Each 9513 contains five counters of 16 bits each. Associated with each counter are an input source, a count register, a load register, a hold register, an output and a gate. The 9513 is extremely flexible and this flexibility can make it a challenge to program the chip directly.

Unlike an Intel 8254 which has a single source, single gate and unique I/O address for each counter, the 9513 is fully programmable and any counter may be internally connected to any gate and receive it's counts from a number of sources. In addition, each counter does not have a unique I/O address. The 9513 takes only two address per chip, one of which is a data path to the counter's load and hold registers.

There is no 9513 register information in this manual. Those wishing to know more about the AM9513 and its programming should request the manual from our technical support group. As of this writing there is no charge for the manual.

We strongly suggest that you use the Universal Library, rather than resort to programming the 9513 directly. It is difficult to program and because programming support is available through the Universal Library, we cannot help with other 9513 programming

The CIO-CTR##HD is an I/O mapped expansion board. The CIO-CTR20HD occupies eight I/O addresses and the CIO-CTR10HD occupies four addresses.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Most of the functions that this board is capable of performing can be acheived using the Universal Library. Unless you have a good reason for direct register manipulation, we suggest you use the Universal Library.

The register descriptions follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

In summary form, the registers and their function are listed on the following table. Within each register are eight bits which may constitute a byte of data or eight individual bit functions.

Table 5-1. Register Functions

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE +0	Data from 9513 #1	Data for 9513 #1
BASE +1	Status of 9513 #1	Commands to 9513 #1
BASE +2	Data from 9513 #2	Data for 9513 #2
BASE +3	Status of 9513 #2	Commands to 9513 #2
BASE +400h	No read function.	Wait State, Interrupt and Counter Source for 9513 #1 and 9513 #2 (1st ten channels on P1)
	Additional for CTR20 only	
BASE +4	Data from 9513 #3	Data for 9513 #3
BASE +5	Status of 9513 #3	Commands to 9513 #3
BASE +6	Data from 9513 #4	Data for 9513 #4
BASE +7	Status of 9513 #4	Commands to 9513 #4
BASE +401h	No read function.	Wait State, Interrupt and Counter Source for 9513 #3 and 9513 #4 (2nd ten channels on P2)

9513 #1 (U1) is accessed at the bottom half of P1 (pins 1 - 22);
 9513 #2 (U2) is the top half of P1 (pins 27 - 48);
 9513 #3 (U3) is accessed at the bottom half of P2 (pins 1 - 22);
 9513 #4 (U4) is the top half of P2 (pins 27 - 48).

5.2 BASE +400 hex & BASE +401 hex

BASE + 400 controls the clock source, interrupt level and wait state for 9513 #1 and 9513 #2

D7	D6	D5	D4	D3	D2	D1	D0
WSEN	CLK11	CLK10	CLK01	CLK00	L2	L1	L0

BASE +401 controls the clock source, interrupt level and wait state for 9513 #3 and 9513 #4

D7	D6	D5	D4	D3	D2	D1	D0
WSEN	CLK11	CLK10	CLK01	CLK00	L2	L1	L0

Read - No read function for these registers.

Write - L0, L1, and L2 select IRQ as follows:

Table 5-2. IRQ Select Codes

L2	L1	L0	IRQ
0	0	0	N/A
0	0	1	N/A
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

For BASE +400, CLK0# selects the clock source for 9513 #1 (the chip designated “U1”), CLK1# selects the clock source for 9513 #2 (the chip designated “U2”)

For BASE +401, CLK0# selects the clock source for 9513 #3 (the chip designated “U3” for the CIO-CTR20HD), CLK1# selects the clock source for 9513 #4 (the chip designated “U4” for the CIO-CTR20HD).

Table 5-3. Clock-Select Codes

CLK#1	CLK#0	CLOCK SOURCE
0	0	1 MHz
0	1	5 MHz
1	0	External
1	1	N/A

WSEN enables or disables the wait state.

1 = Wait State Enabled

0 = Wait State Disabled

*NOTE: **Base +400** applies to CTR10HD and the first ten channels of CTR20 HD. **Base +401** applies to CTR20HD only and the second ten channels.*

6 SPECIFICATIONS

Typical for 25°C unless otherwise specified.

POWER CONSUMPTION

+5V

CIO-CTR10HD	475mA typical, 590mA max
CIO-CTR20HD	800mA typical, 1A max

COUNTER SECTION

Counter type 9513

Configuration

CIO-CTR10HD	Two 9513 devices. 5 counters per 9513, 16 bits each
CIO-CTR20HD	Four 9513 devices. 5 counters per 9513, 16 bits each

Clock input frequency 7Mhz max

X2 Clock input source 1MHz (10MHz Xtal divided by 10), 5MHz (10MHz Xtal divided by 2) or external; software selectable

High pulse width (clock input) 70ns min

Cycle time (clock input) 145ns min

Gate pulse duration 145ns min

Input low voltage -0.5V min, 0.8V max

Input high voltage 2.2V min, 5V max

Output low voltage 0.4V max @ 3.2mA

Output high voltage 2.4V min @ -200µA

Crystal oscillator clock source 10MHz

Frequency accuracy

CIO-CTR##HD 100ppm

CIO-CTR##HD/H50 50ppm

DIGITAL I/O

Interrupts 2 - 7, software selectable

Interrupt enable Programmable

Interrupt sources External

ENVIRONMENTAL

Operating temperature range 0 to 50°C

Storage temperature range -20 to 70°C

Humidity 0 to 90% non-condensing

7 ELECTRONICS AND INTERFACING

7.1 VOLTAGE DIVIDERS

An alternative method of measuring a signal which varies over a range greater than the input range of a digital input, is to use a voltage divider. When correctly designed, it can drop the voltage of the input signal to a safe level the digital input can accept.

Ohm's law states:

$$\text{Voltage} = \text{Current} \times \text{Resistance}$$

Kirkoff's law states:

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

In a voltage divider, the voltage across one resistor in a series circuit is proportional to the total resistance divided by the one resistor (see formula below).

The object in a voltage divider is to choose two resistors having the proportions of the maximum voltage of the input signal to the maximum allowed input voltage.

The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation (A) is 2:1 or just 2.

$$R1 = (A-1) \times R2$$

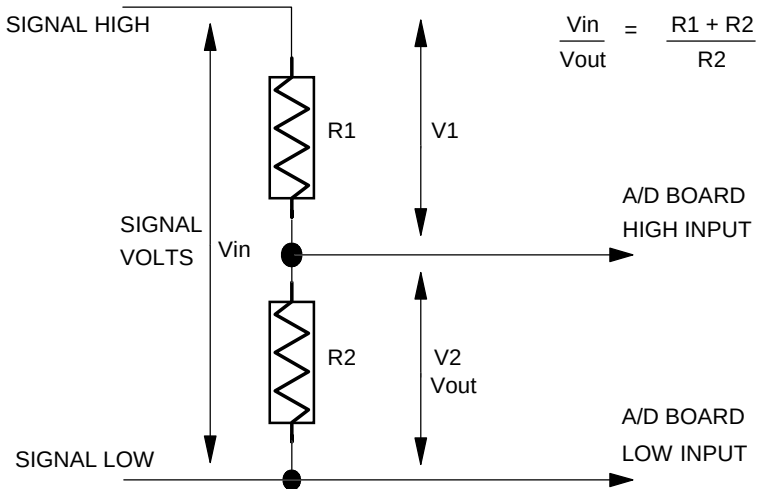
For a given attenuation, pick a resistor and call it R2, then use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to a digital input. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8.

Using the equation above, if R2 is 1K, $R1 = (4.8-1) \times 1000 = 3.8K$.

Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

NOTE



SIMPLE VOLTAGE DIVIDER

The resistors, R1 and R2, are going to dissipate power in the divider circuit according to the equation $W = I^2 \times R$; (Current (I) = Voltage/Resistance). The higher the value of the resistance ($R_1 + R_2$), the less power dissipated by the divider circuit. Here is a simple rule:

For attenuation of $<5:1$, no resistor should be less than 10K.

For attenuation of $> 5:1$, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

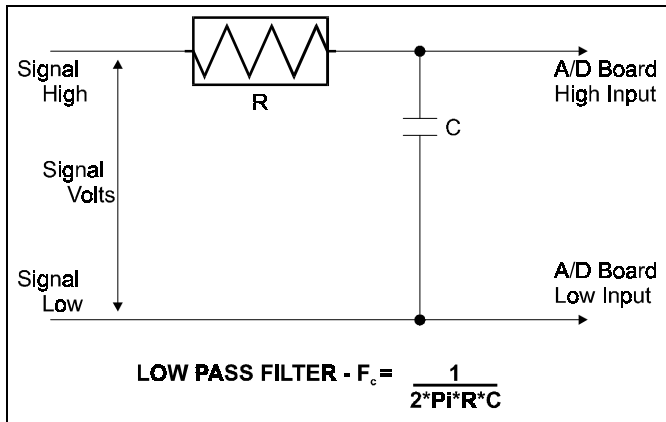
7.2 LOW PASS FILTERS DE-BOUNCE INPUTS

A low pass filter is placed on the signal wires between a signal and an A/D board. It prevents frequencies greater than the cut-off frequency from entering the A/D board's digital inputs.

The cut-off frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low-pass filter had a cut-off frequency of 30 Hz, interference associated with line voltage (60 Hz) would be mostly filtered out but a signal of 25 Hz would pass with less attenuation.

Also, in a digital circuit, a low-pass filter is often used to remove contact bounce noise signals from a switch or a relay contacts. Also, in a digital circuit, a low pass filter might be used to “de-bounce” (filter) an input from a switch or external relay. (Unless switch/relay contacts are mercury-whetted, they tend to bounce briefly on closure, generating a pulsating noise signal. This can easily lead to erroneous counts unless filtered out.)

A simple low-pass filter can be constructed from one resistor (R) and one capacitor (C). The cut-off frequency is determined according to the formula:



$$F_c = \frac{1}{2 \pi R C}$$

Where $\pi = 3.14...$

R = ohms

C = farads

F_c = cut-off frequency in cycles/second

$$R = \frac{1}{2 \pi C F_c}$$

For your notes.

For your notes.

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

CIO-CTR10HD	Counter / Timer Board
CIO-CTR20HD	Counter / Timer Board
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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