

CIO-CTR05 & CIO-CTR10

User's Manual



**MEASUREMENT
COMPUTING™**

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MEGA-FIFO, the CIO prefix to data acquisition board model numbers, the PCM prefix to data acquisition board model numbers, PCM-DAS08, PCM-D24C3, PCM-DAC02, PCM-COM422, PCM-COM485, PCM-DMM, PCM-DAS16D/12, PCM-DAS16S/12, PCM-DAS16D/16, PCM-DAS16S/16, PCI-DAS6402/16, Universal Library, *InstaCal*, *Harsh Environment Warranty* and Measurement Computing Corporation are registered trademarks of Measurement Computing Corporation.

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1 INTRODUCTION

The CIO-CTR10 is really a single board with two CIO-CTR05's on it. For the balance of this manual we will refer to both boards as the CIO-CTR, and will only use the complete board name in instances where there are items specific to one board or the other.

The CIO-CTR family is fully supported by the powerful Universal Library package. Details regarding installation and usage of the Universal Library software can be found in the Universal Library documentation. Please note that InstaCal (shipped with the board) creates a configuration file required for programmers who use the Universal Library programming libraries.

2 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *InstaCal*[™] program provided as part of your software package. *InstaCal*[™] will show you all available options, how to configure the various switches and jumpers (as applicable) to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *InstaCal*[™]. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *InstaCal*[™] and/or your computer.

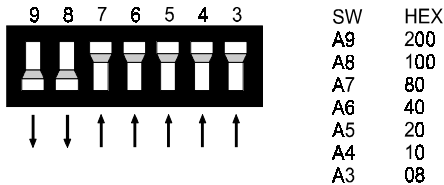
2 HARDWARE INSTALLATION

We highly recommend that you use the InstaCAL procedure to guide you through setting up your board. However, the following sections are provided in case you need to set up your board and you do not have access to the InstaCAL program.

The CIO-CTR has one bank of switches, a base address switch, and one jumper block which must be set before installing the board in your computer.

2.1 BASE ADDRESS

Unless there is already a board in your system which uses address 300h (768 Decimal) then you can leave the switches as they are set at the factory.



In the example shown here, the CIO-CTR is set for base address 300h (768 Decimal).

BASE ADDRESS SWITCH - Address 300H shown here.

Certain address are used by the PC, others are free and may be used by the CIO-CTR and other expansion boards. We recommend BASE = 300h (768D) be tried first.

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-CTR BASE switch may be set for address in the range of 000-3F8 (000-3FC for the CIO-CTR05) so it should not be hard to find a free address area for your CIO-CTR. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use.

Address not specifically listed, such as 390-39F, are usually free.

2.2 INTERRUPT LEVEL SELECT

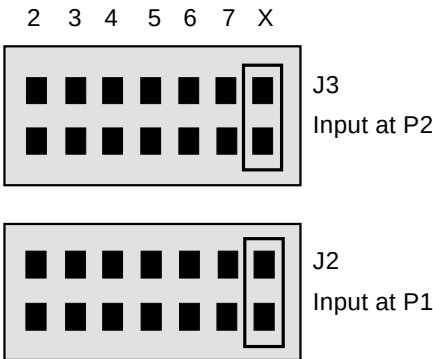
There are two rows of jumper blocks on the CIO-CTR10 and one on the CIO-CTR05, located just above the PC bus interface (gold pins). The factory default setting is that no interrupt level is set. The jumper is in the 'X' position.

Please leave the jumper in the 'X' position for now. Interrupts are hardware initiated software routines and are described in the section on programming.

On the CIO-CTR10 the lower block, J2, is for the IR input on P1. The upper block, J3, is for the IR input on P2

The trigger logic on the CIO-CTR is quite simple. Pin 1 of the 37 pin connector is an input jumper which maps the interrupt directly onto the PC bus. The signal to the bus is buffered. The buffer is enabled by a TTL low level on Pin 2, interrupt enable.

The interrupt level jumper on the CIO-CTR must also be installed. Move it from the 'X' position to the IRQ number you want the interrupt pulse on. On the CTR10, jumper block J2 is associated with the signals on connector P1. Jumper block J3 is associated with the signals on connector P2. Hardware interrupts (assigned by the PC), may be available.



CIO-CTR INTERRUPT JUMPER BLOCK - IRQ Level. The jumper is in the X position which equals no IRQ.

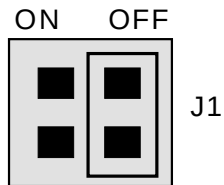
NAME	DESCRIPTION	NAME	DESCRIPTION
NMI	PARITY	IRQ8	REAL TIME CLOCK (AT)
IRQ0 (AT)	TIMER	IRQ9	RE-DIRECTED TO IRQ2
IRQ1	KEYBOARD	IRQ10	UNASSIGNED
IRQ2	RESERVED (XT) INT 8-15 (AT)	IRQ11	UNASSIGNED
IRQ3	COM OR SDLC	IRQ12	UNASSIGNED
IRQ4	COM OR SDLC	IRQ13	80287 NUMERIC CO-P
IRQ5	HARD DISK (AT) LPT (AT)	IRQ14	HARD DISK
IRQ6	FLOPPY DISK	IRQ15	UNASSIGNED
IRQ7	LPT		

IRQ8-15 are AT only.

2.3 WAIT STATE JUMPER

The CIO-CTR boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-CTR is only active when the CIO-CTR is being accessed. Your PC will not be slowed down in general by using the wait state.



WAIT STATE JUMPER BLOCK - For a wait state, place the jumper on the two leftmost pins. No wait state is selected here.

We recommend that the wait state be used in all 16MHz or faster PCs.

2.4 INSTALLING THE CIO-CTR IN THE COMPUTER

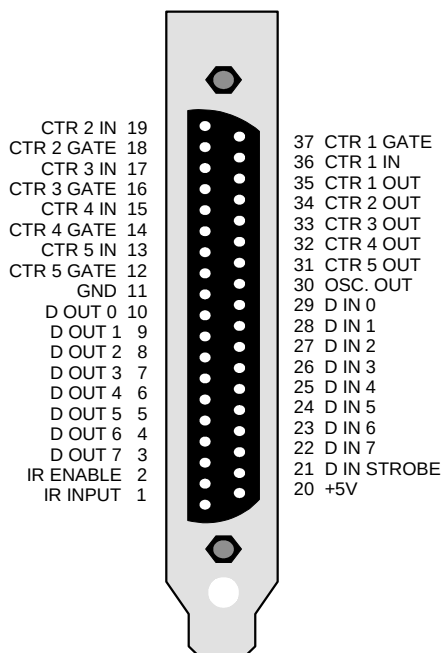
Turn the power off. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed in your computer as you slide the cover off.

Locate an empty expansion slot in your computer. If you are installing a CIO-CTR10, it is best to locate two slots side by side. If you can create two side by side by moving boards, do so.

From the rear of the computer, place the CIO-CTR10 in the right hand of the two empty slots. This means that the empty slot is on the component side of the CIO-CTR. Cabling will be easier if there is an empty slot on the component side of the board.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-CTR. The CIO-CTR connector is a male 37-pin D-type connector. All the signals from the 9513, digital input, digital output and interrupt are accessible. The CTR10 has two of these connectors, P1 and P2. The signals on both are identical.

3 I/O CONNECTOR & PINOUT



CIO-CTR CONNECTOR - View from the rear of the PC.

3.1 CIO-CTR10 SECOND 9513

The CIO-CTR10 has two 9513 chips on it. The second of these, the one accessible via connector P2 at the rear of the board, is wired up identically to the 9513 on P1. Both are Keithley/MetraByte CTM-05 compatible both at the connector and the register level. Software written for the CTM-05, including Labtech Notebook, HP VEE and other third party software can operate both 'CTM-05s'. Simply install one CTM-05 at the BASE ADDRESS and install the other at the BASE ADDRESS + 4.

On the CIO-CTR10, the second 9513 counter timer chip's address is fixed at the board's base address + 4. If the board were configured at 300H (768 Decimal), then the second 9513 would reside at 304h (772 Decimal). No switches need to be set.

4 REGISTER ARCHITECTURE

4.1 CONTROL & DATA REGISTERS

The CIO-CTR10 is composed of 2 AM9513 counter timer chips. The CIO-CTR05 contains one 9513. Each 9513 contains five counters of 16 bits each. Associated with each counter are an input source, a count register, a load register, a hold register, an output and a gate. The 9513 is extremely flexible and this flexibility can make it a challenge to program the chip directly.

Unlike an Intel 8254 which has a single source, single gate and unique I/O address for each counter, the 9513 is fully programmable and any counter may be internally connected to any gate and receive its counts from a number of sources. In addition, each counter does not have a unique I/O address. The 9513 takes only two address per chip, one of which is a data path to the counter's load and hold registers.

There is no 9513 register information in this manual. Those wishing to know more about the AM9513 and its programming should request the manual from our technical support group. As of this writing there is no charge for the manual.

However, we suggest that you use the Universal Library, rather than resort to programming the 9513 directly. It is difficult to program and because programming support is available through the Universal Library, we cannot help with other 9513 programming.

4.2 CIO-CTR10 & CIO-CTR05 ADDRESSES

The CIO-CTR is an I/O mapped expansion board. The CTR10 occupies eight I/O addresses and the CTR05 occupies four addresses.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Most of the functions that this board is capable of performing can be achieved using the Universal Library. Unless you have a good reason for direct register manipulation, we suggest you use the Universal Library.

The register descriptions follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on the following table. Within each register are eight bits which may constitute a byte of data or eight individual bit functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE +0	Data from 9513 #1	Data for 9513 #1
BASE +1	Status of 9513 #1	Commands to 9513 #1
BASE +2	Digital input port, P1	
BASE +3	No read back of output port	Digital output port
	CTR 10 ONLY	
BASE +4	Data from 9513 #2	Data for 9513 #2
BASE +5	Status of 9513 #2	Cammands to 9513 #2
BASE +6	Digital input port, P2	
BASE +7	No read back of output port	Digital output port, P2

4.3 DIGITAL I/O REGISTERS

The digital input port at BASE + 2 is a 74LS373 input buffer with a strobe line. When STROBE is high, the current status of the inputs to the 74LS373 may be read. When STROBE goes low, the 74LS373 inputs are latched.

The digital output port at $\text{BASE} + 3$ is a 74LS273 output buffer. Each write to $\text{BASE} + 3$ places a byte of data on the output port.

5 SPECIFICATIONS

Typical for 25°C unless otherwise specified.

POWER CONSUMPTION

+5V	
CIO-CTR10	300mA typical, 500mA max
CIO-CTR05	190mA typical, 320mA max

COUNTER SECTION

Counter type	9513
Configuration	
CIO-CTR10	Two 9513 devices. 5 counters per 9513, 16 bits each
CIO-CTR05	One 9513 device. 5 counters, 16 bits each
Clock input frequency	7Mhz max
X2 Clock input source	1MHz (10MHz Xtal divided by 10)
High pulse width (clock input)	70ns min
Cycle time (clock input)	145ns min
Gate pulse duration	145ns min
Input low voltage	-0.5V min, 0.8V max
Input high voltage	2.2V min, 5V max
Output low voltage	0.4V max @ 3.2mA
Output high voltage	2.4V min @ -200μA
Crystal oscillator clock source	10MHz
Frequency accuracy	
CIO-CTR##	100ppm
CIO-CTR##/H50	50ppm

DIGITAL I/O

Digital Type

Output: 74LS273

Input: 74LS373

Configuration 2 banks of 8: 1 bank input, 1 bank output,
input may be latched via external strobe input
(latched on TTL low level)

Number of channels 8 input, 8 output

Output High 2.7 volts min @ -0.4mA

Output Low 0.5 volts max @ 8 mA

Input High 2.0 volts min, 7 volts absolute max

Input Low 0.8 volts max, -0.5 volts absolute min

Interrupts

2 - 7, jumper selectable

Interrupt enable

External, enabled with TTL low level

Interrupt sources

External

ENVIRONMENTAL

Operating temperature range 0 to 50°C

Storage temperature range -20 to 70°C

Humidity 0 to 90% non-condensing

6 ELECTRONICS AND INTERFACING

6.1 VOLTAGE DIVIDERS

An alternative method of measuring a signal which varies over a range greater than the input range of a digital input, is to use a voltage divider. When correctly designed, it can drop the voltage of the input signal to a safe level the digital input can accept.

Ohm's law states:

$$\text{Voltage} = \text{Current} \times \text{Resistance}$$

Kirkoff's law states:

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

In a voltage divider, the voltage across one resistor in a series circuit is proportional to the total resistance divided by the one resistor (see formula below).

The object in a voltage divider is to choose two resistors having the proportions of the maximum voltage of the input signal to the maximum allowed input voltage.

The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation (A) is 2:1 or just 2.

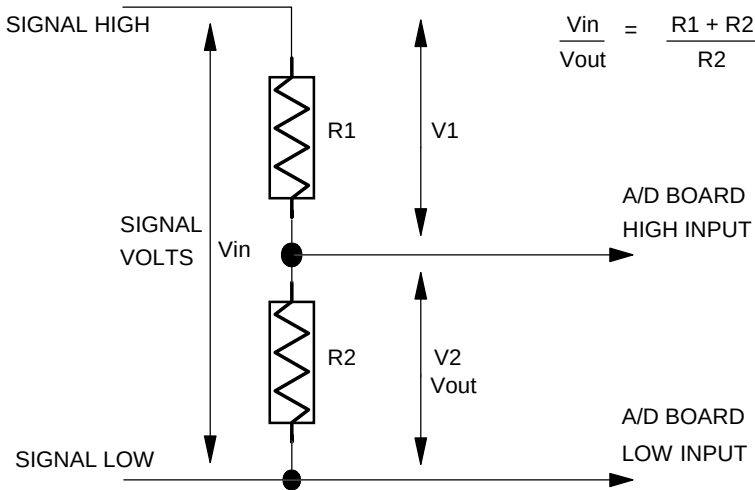
$$R1 = (A-1) \times R2$$

For a given attenuation, pick a resistor and call it R2, the use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to a digital input. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8.

Using the equation above, if R2 is 1K, $R1 = (4.8-1) \times 1000 = 3.8K$.

Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.



NOTE

The resistors, R1 and R2, are going to dissipate power in the divider circuit according to the equation $W = I^2 \times R$; (Current (I) = Voltage/Resistance). The higher the value of the resistance (R1 + R2), the less power dissipated by the divider circuit. Here is a simple rule:

For attenuation of <5:1, no resistor should be less than 10K.

For attenuation of > 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. It is a 16" by 4" screw terminal board with two 37-pin D-type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall, or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with components for your application.

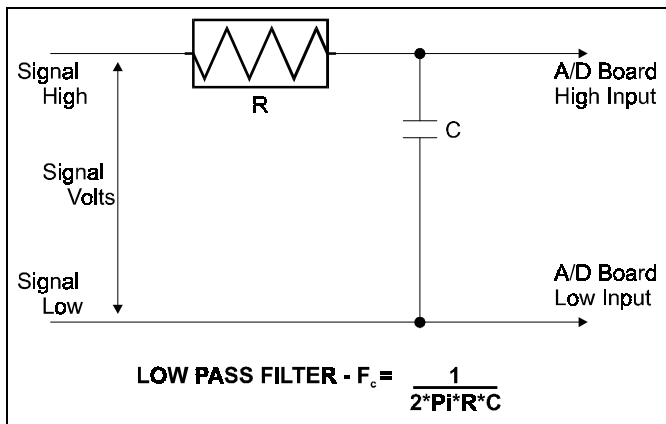
6.2 LOW PASS FILTERS DE-BOUNCE INPUTS

A low pass filter is placed on the signal wires between a signal and an A/D board. It prevents frequencies greater than the cut-off frequency from entering the A/D board's digital inputs.

The cut-off frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low-pass filter had a cut-off frequency of 30 Hz, interference associated with line voltage (60 Hz) would be mostly filtered out but a signal of 25 Hz would pass with less attenuation.

Also, in a digital circuit, a low-pass filter is often used to remove contact bounce noise signals from a switch or a relay contacts. Also, in a digital circuit, a low pass filter might be used to “de-bounce” (filter) an input from a switch or external relay. (Unless switch/relay contacts are mercury-whetted, they tend to bounce briefly on closure, generating a pulsating noise signal. This can easily lead to erroneous counts unless filtered out.)

A simple low-pass filter can be constructed from one resistor (R) and one capacitor (C). The cut-off frequency is determined according to the formula:



$$F_c = \frac{1}{2 \pi R C}$$

Where $\pi = 3.14...$

R = ohms

C = farads

Fc = cut-off frequency in cycles/second

$$R = \frac{1}{2 \pi C F_c}$$

For your notes.

EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

CIO-CTR05	5 channel counter/timer board
CIO-CTR10	10 channel counter/timer board
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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